FINAL EXAM
SECOND SEMESTER SESSION 2011/2012

COURSE CODE / NAME : STIK2023 / COMPUTER SYSTEM ARCHITECTURE
DATE : 26 JUNE 2012 (TUESDAY)
TIME : 2:30 P.M. – 5:00 P.M. (2 ½ HOURS)
VENUE : DMS

INSTRUCTION :

1. Answer ALL questions in the answer spaces provided.
2. You are allowed to use scientific calculator.
3. This booklet contains FOURTEEN (14) questions in NINE (9) printed pages excluding the cover page.

MATRIC NO : ____________________________  (with word)  ____________________________  (with number)
IDENTIFICATION CARD NO. :
LECTURER : ____________________________
GROUP :  ______  TABLE NO. :  __________

DO NOT OPEN THIS EXAMINATION PAPER UNTIL INSTRUCTED

CONFIDENTIAL
STIK 2023 Computer System Architecture

1. Computer architecture deals with the functional behavior of a computer system.
   a. List down the FIVE (5) major components of the computer as defined in the von Neumann model.

   (5 Marks)

   b. Draw a diagram to show how all the components are interrelated.

   (3 Marks)
2. Give value for the following base conversion and show your work.
   
a. \(14.75_{10}\) to base 2

\[\text{3 Marks}\]

b. \(89_{10}\) to base 8

\[\text{3 Marks}\]

c. \(10011011_{2}\) to base 16

\[\text{3 Marks}\]

3. Convert the following numbers as indicated.
   
a. \(110101_{2}\) to unsigned base 10.

\[\text{3 Marks}\]

b. \(-29_{10}\) to 2's complement (use 8 bits in the result).

\[\text{3 Marks}\]
c. 61543_8 to unsigned base 16 (use four base 16 digits in the result).  

(3 Marks)

d. 37_{10} to unsigned base 3 (use four base 3 digits in the result).  

(3 Marks)

4. Karnaugh Map is one of the methods used to simplify the Boolean expression.  
Given,  
\[ F(A,B,C,D) = \Sigma(0,5,7,8,9,10,11,13,15) \]  
\[ d(A,B,C,D) = \Sigma(1,2,3,4) \]

a. Draw a Karnaugh Map and fill in the cells with 1 and X (don’t care), and simplify it using group.  

(4 Marks)

b. Get the simplified Boolean expression.  

(3 Marks)
c. Draw the logic circuit. (3 Marks)

5. Construct a 16-to-1-line multiplexer with TWO (2) 8-to-1-line multiplexers and ONE (1) 2-to-1-line multiplexer. Use block diagrams for the three multiplexers. (7 Marks)
6. Show the results of adding/subtracting the following pairs of six-bit (i.e. one sign bit and five data bits) two’s complement numbers and indicate whether or not overflow/underflow occurs for each case:

(5 Marks)

\[ \begin{array}{c c c c}
\text{101011} & \text{111111} \\
+ \text{100101} & + \text{000111} \\
\hline
\text{111110} & \text{100001} \\
\hline
- \text{100101} & - \text{011101} \\
\hline
\end{array} \]

7. Write a program fragment using ld, st and add instructions in assembly language format for the statement:

\[ z = x + y; \]

(5 Marks)
8. Give the definitions of:
   a. Data bus (2 Marks)
   b. Address bus (2 Marks)
   c. Control bus (2 Marks)
   d. Power bus (2 Marks)

9. List the microinstructions that are executed in interpreting the ARC "$s1, %r2, %r3$" instruction. Start with microinstruction 0. Only list the microinstruction numbers, and not the code. (4 Marks)
10. Give **FIVE (5)** characteristics of Reduced Instruction Set Computer (RISC) architecture that distinguish them from Complex Instruction Set Computer (CISC).

(5 Marks)

11. Static RAM (SRAM) and Dynamic RAM (DRAM) are two types of Random Access Memory (RAM). Explain briefly.
   a. SRAM

(3 Marks)

b. DRAM

(3 Marks)
12. Discuss briefly the hardware schemes that have been developed for translating main memory addresses to cache memory addresses:
   a. Associative Mapped Cache

   (3 Marks)

   b. Direct-Mapped Cache

   (3 Marks)

   c. Set-Associative Mapped Cached

   (3 Marks)
13. Compute the storage capacity of a hard disk, C, with the following information:
   Number of bytes per sector, \( N = 512 \) bytes
   Number of sectors per track, \( S = 1,000 \) sectors
   Number of tracks per surface, \( T = 30,000 \) tracks
   Number of data encoded platter surfaces, \( P = 8 \) platters surfaces

   (6 Marks)

14. According to Amdahl's law in measuring the performance of a computer, the speedup is expressed in terms of the number of the processors and the fraction of operations that must be performed sequentially. Given there are 10 processors and the fraction of operations is 10%, calculate the speedup.

   (6 Marks)

END OF QUESTIONS